IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Won Sun Shin et al.		
Assignee:	Amkor Technology, Inc.		
Title:	SEMICONDUCTOR PACKAGE AND METHOD FOR FABRICATING THE SAME		
Serial No.:	10/825,670	Filing Date:	April 14, 2004
Patent No.:	RE40,112	Issued:	February 26, 2008
Examiner:	Chuong A. Luu	Group Art Unit:	2818
Docket No.:	GK0012RI		

Monterey, CA
October 9, 2008

ATTENTION: CERTIFICATE OF CORRECTIONS BRANCH
COMMISSIONER FOR PATENTS
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REQUEST FOR ENTRY OF CERTIFICATE OF CORRECTION

Sir:

Please enter the enclosed Certificate of Correction (PTO Form 1050) in the above patent.

The errors sought to be corrected were made by

[X] The Patent and Trademark Office as explained below. Thus, no fee is required for the Certificate of Correction pursuant to 37 CFR §1.322.

[ ] Applicant(s) (at least in part). See next section for explanation. This appropriate fee under 37 CFR §1.323 has been authorized below.

Attached as Exhibit A (3 pages) is a copy of the relevant pages of the Claims as filed with the original application on May 19, 2000, which supports the requested correction to Claims 3, 19 and 26 and shows that the errors were made by the U.S. Patent and Trademark Office.

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As shown in Exhibit A, Line 14 of Claim 3 reads "...ones of the first ball lands". The same line in the patent at Column 13, Line 49 reads "...ones of the ball lands". Specifically, the word "first" was incorrectly omitted from the Claim.

As also shown in Exhibit A, Line 3 of Claim 19 reads "...all of the unit circuit boards...". The same line in the patent at Column 15, Line 3 reads "...all of the unit circuit board...". Specifically, the word "board" should be replaced with the word --boards--.

As further shown in Exhibit A, Line 4 of Claim 26 reads "...one of which has cavities and gates...". The same line in the patent at Column 16, Line 10 reads "...one or which has cavities and gates...". Specifically, the word "or" should be replaced with the word --of--.

The Commissioner is hereby authorized to charge any fees required for consideration and entry of the enclosed documents, and to credit any overpayment of fees to Deposit Account No. 50-0553.

Please direct all inquiries concerning this request to the undersigned attorney.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 9, 2008.

Attorney for Applicant(s) — October 9, 2008 Date of Signature

Respectfully submitted,

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3. The method of claim 1, wherein the circuit board strip comprises:

a resin substrate having a substantially rectangular strip shape provided with a first major surface and a second major surface;

a plurality of slots extending to a desired length and serving to divide each of the resin substrate into a plurality of substrate portions arranged in a matrix array, each of the substrate portions corresponding to one of the unit circuit boards having one of the through holes;

a plurality of first circuit patterns each formed on the first major surface of the resin substrate for an associated one of the strip portions and provided with associated ones of the first ball lands;

a plurality of second circuit patterns each formed on the second major surface of the resin substrate for an associated one of the strip portions and provided with associated ones of the bond fingers; and

cover coats respectively coated over the first and second major surfaces of the resin substrate while allowing the bond fingers and the ball lands to be exposed therethrough.

4. The method of claim 1, further comprising attaching one or more closure members to the first surface of the substrate strip so that each through hole is covered thereby prior to receiving the semiconductor chip in the respective through hole.

Exhibit A 30

18. The method according to claim 5, wherein a unitary body of encapsulant material covers the second major surface of all of the unit circuit boards of the circuit board strip.

19. The method according to claim 6, wherein a unitary body of encapsulant material covers the second major surface all of the unit circuit boards of the circuit board strip.

20. The method according to claim 17, wherein singulating the circuit board strip is carried out in such a fashion that the encapsulant material and the circuit board strip are simultaneously split.

21. The method according to claim 18, wherein singulating the circuit board strip is carried out in such a fashion that the encapsulant material and the circuit board strip are simultaneously split.

22. The method according to claim 19, wherein singulating the circuit board strip is carried out in such a fashion that the encapsulant material and the circuit board strip are simultaneously split.

23. The method of claim 1, wherein encapsulating the circuit board strip comprises:

into the cavity; and

injecting the encapsulating material into each of the cavities through the associated gate in such a fashion that it flows outwardly from a central portion of the second major surface of the associated semiconductor chip along the second major surface, fills the through hole, and contacts the closure member.

26. The method of claim 9, wherein the encapsulating the circuit board strip comprises:

interposing the circuit board strip between a pair of mold dies, one of which has cavities and gates, in such a fashion that the second major surface of each of the semiconductor chips faces an associated cavity and a gate into the cavity; and

injecting the encapsulating material into each of the cavities through the associated gate in such a fashion that it flows outwardly from a central portion of the second major surface of the associated semiconductor chip along the second major surface, fills the through hole, and contacts the closure member.

27. The method of claim 1, wherein each unit circuit board of the circuit board strip is further provided with a plurality of second ball lands at the second major surface thereof.

28. The method of claim 2, wherein each unit circuit board of the circuit board strip is further provided with a

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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : RE40,112

APPLICATION NO. : 10/825,670

ISSUE DATE : February 26, 2008

INVENTOR(S) : Won Sun Shin, Do Sung Chun, Sang Ho Lee, Seon Goo Lee and Vincent Dicaprio

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 13, Line 49, Claim 3, replace "ones of the ball lands" with --ones of the first ball lands--;
In Column 15, Line 3, Claim 19, replace "the unit circuit board" with --the unit circuit boards--;
In Column 16, Line 10, Claim 26, replace "one or which" with --one of which--.

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